UNITED STATES PATENT AND TRADEMARK OFFICE

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10/556,450	11/10/2005	Chee Yu Ng	NL 030575	3813

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ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-12 are pending and have been examined.

2.   Claims 1-12 are rejected.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.   Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Independent claims 1 and 10 recite a "first interface for connection to a memory bus...such that the host controller is adapted to act only as a slave on the memory bus" and "wherein the host controller is adapted to:...copy the updated stored transfer-based transfer descriptors to the system memory" which is indefinite because it is unclear how, with the information provided in the claims and originally filed specification, a host controller can copy information to the system memory on the memory bus without being a bus master.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1-12 are rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(b) as being

anticipated by Wang et al. (US Patent Application Publication No. 2002/0116565).

For claim 1 Wang discloses:

A host controller (Fig. 1A, 100), for use in a bus communication device comprising a host

microprocessor and a system memory, the host controller comprising:

- a first interface (Fig. 1A, the left side of host controller 100) for connection to a memory

  bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system

  memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the

  memory bus ([0138-0140] describe how the host controller is not required to act as a bus

  master);

- an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer

  descriptors received through the first interface ([0041]); and

- a second interface (Fig. 1A, 28 the right side of host controller), for connection to an

  external bus (Fig. 1A, the lines connecting to USB devices 26),

- wherein the host controller is adapted to:

    o   execute stored transfer-based transfer descriptors ([0041-0042]);

    o   update the content of the stored transfer-based transfer descriptors on execution

        ([0051] "...and updates, in state 76, a record in the transaction descriptor..."); and

    o   copy the updated stored transfer-based transfer descriptors to the system memory

        ([0138-0140] describes the processes of where the host controller transfers data to

        the system memory under the control of the microprocessor).

For claim 2 Wang discloses:

A host controller as claimed in claim 1, wherein the internal memory is a dual-port RAM ([0054]).

For claim 3 Wang discloses:

A host controller as claimed in claim 1, wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously ([0056] "The batch memory 30 is preferably organized as to be able to receive USB transactions from the host microprocessor 24 for one batch while the host controller system 100 is acting on another batch.").

For claim 4 Wang discloses:

A host controller as claimed in claim 1, wherein the internal memory is divided into two parts (Fig. 5, first part 106 and second part 116), and is adapted to store transfer-based transfer descriptor headers in a first part ([0060]), and to store transfer-based transfer descriptor payload data in a second part ([0063]).

For claim 5 Wang discloses:

A host controller as claimed in claim 4, wherein the first part of the internal memory is sub-divided into two sub-parts, and is adapted to store transfer descriptor headers relating to periodic transfers in a first sub-part ([0062,0065] "isochronous transaction"), and to store transfer

descriptor headers relating to asynchronous transfers in a second sub-part ([0065] "bulk

transaction"]).

For claim 6 Wang discloses:

A host controller as claimed in claim 5, wherein the host controller is adapted to scan the first

sub-part of the internal memory once in each micro-frame ([0065] "For example, five

transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous of 1023 and

four bulk or interrupt transactions of 64 bytes each." The host controller therefore scanned the

control memory [CM] once in the micro-frame thus meeting the claim limitation.), and is

adapted to scan the second sub-part continuously throughout each micro-frame ([0065] "For

example, five transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous

of 1023 and four bulk or interrupt transactions of 64 bytes each." The host controller therefore

scanned the control memory [CM] throughout the micro-frame thus meeting the claim

limitation.).

For claims 7 and 11 Wang discloses:

A host controller as claimed in claim 1, wherein the host controller is a USB host controller and

the second interface is a USB bus interface (Fig. 1A, [0003, 0016]).

For claims 8 and 12 Wang discloses:

A host controller as claimed in claim 1, wherein the internal memory is adapted to store multiple

micro-frames of transfer descriptors ([0056] "The batch memory 30 is preferably organized so as

to be able to receive USB transactions from the host microprocessor 24 for one batch while the

host controller system 100 is acting on another batch."), and to execute the stored transfer

descriptors without intervention from the host microprocessor ([0042] describes how the host

controller executes the stored transfer descriptors without the microprocessor.).

For claim 9 Wang discloses:

A host controller as claimed in claim 8, wherein each of the multiple micro-frames of transfer

descriptors may store payload data relating to one or more of isochronous, interrupt and bulk

data transfers ([0063, 0070] describe a data memory 116 [Fig. 5] holds data for USB transactions

of type isochronous, bulk or interrupt [0062,0065].).

For claim 10 Wang discloses:

A bus communication device, comprising:

- a host microprocessor (Fig. 1A, 24);

- a system memory (Fig. 1A, 32);

- a memory bus, which connects the host microprocessor and the system memory (Fig. 1A
  line connecting 24 and 32; and

- a host controller (Fig. 1A, 100), wherein the host microprocessor is adapted to form
  transfer-based transfer descriptors, and write the transfer-based transfer descriptors to the
  system memory and to the host controller, and wherein the host controller comprises:

  o a first interface (Fig. 1A, the left side of host controller 100) for connection to a
    memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24)

and the system memory (Fig. 1A, 32), such that the host controller is adapted to

act only as a slave on the memory bus ([0138-0140] describe how the host

controller is not required to act as a bus master);

o an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer

descriptors received through the first interface ([0041]); and

o a second interface (Fig. 1A, 28 the right side of host controller), for connection to

an external bus (Fig. 1A, the lines connecting to USB devices 26),

o wherein the host controller is adapted to:

- execute stored transfer-based transfer descriptors ([0041-0042]);

- update the content of the stored transfer-based transfer descriptors on

execution ([0051] "...and updates, in state 76, a record in the transaction

descriptor..."); and

- copy the updated stored transfer-based transfer descriptors to the system

memory ([0138-0140] describes the processes of where the host controller

transfers data to the system memory under the control of the

microprocessor).

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure because it pertains to the transfer of USB data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RMS

PAUL R. MYERS
PRIMARY EXAMINER